REMARKS

This response is filed in furtherance to the after-final response previously filed. As instructed in the transmittal filed herewith, the amendment to claim 12 (filed in that previous amendment) should be entered, and the remarks set forth in that prior submission should be considered. In addition, Applicant submits the further remarks set forth herein.

Applicant appreciates the Examiner's thorough review of the present application, and respectfully requests reconsideration of the rejection set forth in the FINAL Office Action, in light of the previous amendment (now entered) and the following additional remarks. Claims 12-20 remain pending in the application.

Claims 13-20 ultimately depend on amended claim 12, and therefore are considered to be in condition for allowance, for at least the same reasons as claim 12.

The invention defined by claim 12 differs from U.S. Patent 6,610,591 in at least the ways described below. The second part 42 according to the prior art (as represented by Fig. 1 of U.S. Patent 6,610,591) connects the first part 44 instead of contacting the device carrier 10 and the semiconductor unit 20 -- *i.e.*, there is one portion of the first part 44 between the second part 42 and the device carrier 10, and there is another portion of the first part 44 between the second part 42 and the semiconductor unit 20. In contrast, both the first part 3 and the second part 5 of an interconnection portion according to the claimed invention respectively contact the device carrier 7 and the semiconductor unit 2, i.e., the second part 5 according to the claimed invention has one end 57 contacting the device carrier 7 and has another end 58 contacting the semiconductor unit 2. In other words, according to the claimed invention, no material with lower melting point is either located between the second part 5 and the semiconductor unit 2, or located between the second part 5 and the device carrier 7. As a result, the height of the gap between the device

carrier 7 and the semiconductor unit 2 according to the claimed invention depends solely on the size of the second part 5. This is significantly different from the prior art according to which the height of the gap between the device carrier 10 and the semiconductor unit 20 depends on the thickness, softness, and temperature sensitivity (due to lower melting point) of the first part 44 in addition to the size of the second part 42.

Another difference between the claimed invention and the prior art is in the object of these inventions. The object (lines 21-41 of col 2) of the prior art is to provide a solution to a problem resulting from planarity of the substrate and the semiconductor die. In contrast, the embodiment of the present invention claimed in claim 12 provides a solution to a problem (lines 15-19 of page 1): in the conventional art of connecting a chip via bumps to a lead frame or a device carrier having neither connection pads nor insulation layer thereon, a heating (or reflow soldering) process results in bumps' collapses of inconsistent height due to disunity of wetty (or solder flowing) on the surface of such a device carrier because no mechanism is provided to limit the solder flowing. Another objective solved by the embodiment of claim 12 (see e.g., lines 15-20 of page 1) the problem in conventional art of connecting a chip via bumps to a lead frame or a device carrier having neither connection pads nor insulation layer thereon, the chip may contact the device carrier as a result of bumps' collapses of inconsistent height due to disunity of wetting (or solder flowing) on the surface of such a device carrier.

The invention of claim 12 differs from U.S. Patent 6,281,581 in at least the ways described below. The first part 612 and 614 according to the prior art (as represented by Fig. 5A of U.S. Patent 6,281,581) are physically separated but mechanically connected in series by the second part 610 to form an interconnection portion between the device carrier 604 and the semiconductor unit 606, i.e., the interconnection portion according to the prior art is formed by

connecting, in series, one first part 612, the second part 610, and another first part 614. In contrast, both the first part 3 and the second part 5 according to the claimed invention respectively have one end (37, 57) contacting the device carrier 7, and respectively extend therefrom toward the semiconductor unit 2 to respectively have another end (38, 58) contacting the semiconductor unit 2.

Another difference between the claimed invention and the prior art is the area of surface of the second part 610, which is covered/adhered by the first part 612 and 614. The second part 610 according to the prior art has only part of its surface connected to the first part 612 and 614, and thereby is mostly exposed. In contrast, according to the claimed invention, the second part 5 of an interconnection portion between a semiconductor unit 2 and a device carrier 7, except its two ends 57 and 58 which respectively contact the device carrier 7 and the semiconductor unit 2, is covered by the first part 3, and thereby is not exposed.

A further difference between the claimed invention and the prior art is observed in the objects of these inventions. The object of the prior art is to provide a solution to a problem (lines 11-26 of col 2, Fig. 3): a crack 34 resulting from thermal fatigue is formed between a solder joint and a corresponding pad 33 of a device carrier 32. In contrast, the claimed invention provides a solution to a different problem (lines 15-19 of page 1): namely, in conventional arts of connecting a chip via bumps to a lead frame or a device carrier having neither connection pads nor insulation layer thereon, reflow soldering (heat applying) process resulting in bumps' collapses of inconsistent height due to disunity of wetty (or solder flowing) on the surface of such a device carrier, because of the lack of mechanism to limit the solder flowing. Another object of the claimed invention is to solve another problem (lines 15-20 of page 1): namely, in conventional arts of connecting a chip via bumps to a lead frame or a device carrier having

neither connection pads nor insulation layer thereon, the chip may contact the device carrier as a result of bumps' collapses of inconsistent height due to disunity of wetting (or solder flowing) on the surface of such a device carrier.

The invention of claim 12 (one embodiment of which is illustrated in Fig. 6) differs from U.S. Patent 6,506,671 (embodiments of which are illustrated in Figs. 3 and 6 thereof) in at least the ways described below. The second part (solder ball 20') of an interconnection portion between a semiconductor device 10 and a substrate 30 according to the prior art is partially surrounded by the first part (ring 50'), wherein the first part (ring 50') includes aperture 52 and has a melting point higher than that of the second part (solder ball 20'). In contrast, the second part 5 of an interconnection portion between a semiconductor unit 2 and a device carrier 7 according to the claimed invention is surrounded by the first part 3, wherein the first part 3 has a melting point lower than that of the second part 5.

The fact the melting point of the first part (ring 50') according to the prior art is higher than that of the second part (solder ball 20') is established by the following statements cited from its specification: "Since the ring protrudes from the surface of the semiconductor device component, when a solder ball is bonded or otherwise secured to the contact pad exposed through the ring, the ring laterally surrounds at least a portion of the solder ball....." in lines 63-67 of col 3 and lines 1-5 of col 4; "Another significant advantage of the rings of the present invention is the containment of the solder of the balls, in the manner of a dam, during solder reflow, thus preventing contamination of the passivation layer surrounding the contact pads" in lines 17-21 of col 4; "Each ring 50 defines an aperture 52 through which at least a portion of the surrounded contact pad 12 is exposed. Each ring 50 protrudes from surface 14 of semiconductor device 10 so as to laterally surround and contact at least a portion of a solder ball to be bonded or

otherwise secured to bond pad 12 and to support that portion of the solder ball to prevent fatigue thereof during thermal cycling of semiconductor device 10" in lines 45-52 of col 5; "As shown in FIG. 5, solder ball 20' extends through an aperture 52' of ring 50' to contact pad 12" in lines 26-27 of col 6; and "rings 50' prevent material of solder balls 20' from contacting surface 14 of semiconductor device 10" in lines 37-38 of col 6. The melting point of the first part (ring 50') according to the prior art must be higher than that of the second part (solder ball 20') if the statements above are true.

Another difference between the claimed invention and the prior art is the distance between the first part of an interconnection portion and the device carrier. There is a distance between the first part (ring 50') and the device carrier (substrate 30) according to the prior art because the first part (ring 50') is fabricated before the semiconductor device 10 is connected to the substrate 30 via the second part (solder ball 20'). In contrast, both the first part 3 and the second part 5 according to the claimed invention respectively contact the device carrier 7 and the semiconductor unit 2, and there is no distance between the first part 3 and the device carrier 7. This results from the fact that the first part 3 according to the claimed invention is formed in the process of connecting the semiconductor unit 2 with the device carrier 7.

A further difference between the claimed invention and the prior art is that the object of the prior art is to provide a solution to a problem (lines 44-60 of col 1): expansion and contraction resulting from thermal cycling during manufacturing and testing process are serious at the interface between a solder ball and a contact pad of a semiconductor device, causing solder fatigue, reducing the strength of the solder balls, resulting in cracking and failure of the solder balls, and diminishing the reliability of the solder balls as mechanical and electrical connection elements. In contrast, one object of the embodiment recited in claim 12 is to provide a solution

to a problem (lines 15-19 of page 1): in conventional arts of connecting a chip via bumps to a lead frame or a device carrier having neither connection pads nor insulation layer thereon, reflow soldering (heat applying) process always results in bumps' collapses of inconsistent height due to disunity of wetty (or solder flowing) on the surface of such a device carrier, because of the lack of mechanism to limit the solder flowing. Another object of the embodiment of the invention recited in claim 12 is to provide a solution to another problem (lines 15-20 of page 1): in conventional arts of connecting a chip via bumps to a lead frame or a device carrier having neither connection pads nor insulation layer thereon, the chip contacts the device carrier as a result of bumps' collapses of inconsistent height due to disunity of wetting (or solder flowing) on the surface of such a device carrier.

A feature that the second part 5 directly contacts the metal surface 72 and the semiconductor unit 2, and another feature that both the first part and the second part span between and tie together the metal surface and the semiconductor unit, are now added to claim 12. The added features are not anticipated or suggested by the combination of U.S. Patent 6,610,591, U.S. Patent 6,281,581, U.S. Patent 6,506,671, and the prior art of which applicant currently is aware.

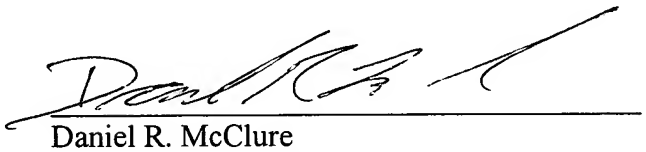
The features included in amended independent claim 12 are neither anticipated nor suggested by the combination of U.S. Patent 6,610,591, U.S. Patent 6,281,581, U.S. Patent 6,506,671, and the prior art of which applicant currently is aware. Accordingly, amended claim 12 overcomes the Examiner's rejections under 35 U.S.C. 102(e) and 103(a), and is in condition for allowance. Claims 13-20 depend on amended claim 12, and all such dependent claims therefore are in condition for allowance and such action is respectfully requested.

CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

By: 

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